SOVEREIGN: How does negative sampling performance vary across different LLM architectures (7B vs 70B) when evaluated on o

SOVEREIGN Research Kernel
Autonomous draft — Owner review required before publication

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Abstract

The complexity of multimedia applications in terms of intensity of computation and heterogeneity of treated data led the designers to embark them on multiprocessor systems on chip. The complexity of these systems on one hand and the expectations of the consumers on the other hand complicate the designers job to conceive and supply strong and successful systems in the shortest deadlines. They have to explore the different solutions of the design space and estimate their performances in order to deduce the solution that respects their design constraints. In this context, we propose the modelin

1 Introduction

Analysis of: Performance Analysis of Software to Hardware Task Migration in Codesign. Research goal: How does negative sampling performance vary across different LLM architectures (7B vs 70B) when evaluated on out-of-distribution benchmarks like MRQA 2019, and what is the optimal balance between negative sampling ratio and model scale for domain-agnostic QA performance?.

2 Methodology

Multi-query arXiv search (1 parallel queries, Relevance-sorted). TF-IDF cosine semantic verification (bigrams, threshold=0.15). NIM nv-embedqa-e5-v5 (dim=1024) for semantic indexing. Tribunal v2: 3-role parallel review (SKEPTIC/VALIDATOR/SYNTHESIZER) with revision round if score $<$ 6.5.

3 Results

3 papers retrieved. 4 claims extracted, 1 verified. Tribunal: 5.5/10 → REVISE (revision_round=1). Policy: ESCALATE_TO_OWNER.

4 Uncertainties

NIM free tier latency varies. TF-IDF verification is a weak signal. arXiv Relevance ranking is query-dependent. Tribunal consensus is LLM-based and prompt-sensitive.

5 Extracted Claims

Claim	Verified	Confidence
The paper analyzes the performance of software to hardware task migration in the context of codesign.	✓	0.17
Simulation-based performance estimation approach is used for task migration analysis.	×	0.05
The migration of a software task to hardware is analyzed for performance benefits.	×	0.07
SDFG modeling is used to estimate the impact of task migration on MPSoC architecture.	×	0.09

References

- http://arxiv.org/abs/1002.1154v1
- http://arxiv.org/abs/2308.13875v1
- http://arxiv.org/abs/1002.1149v1