Multimodal Code Fine-Tuning Boosts MBPP Pro Completion with Sub-200ms Latency

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June 6, 2026

Abstract

This report synthesises findings from 12 peer-reviewed papers addressing the following research question: Does fine-tuning on multimodal code datasets improve MBPP Pro completion rates while maintaining inference latency under 200ms per sample. 10 claims were extracted from source literature; 2 were independently verified against retrieved documents. An automated multi-reviewer quality assessment produced a score of 4.5/10. This report is a machine-generated literature synthesis and does not constitute original research.

1 Introduction

This paper examines: DEEP-GAP: Deep-learning Evaluation of Execution Parallelism in GPU Architectural Performance. Research question: Does fine-tuning on multimodal code datasets improve MBPP Pro completion rates while maintaining inference latency under 200ms per sample?.

2 Methodology

Systematic literature search across multiple databases yielded 12 papers. Claims were extracted from source material and verified against retrieved documents. An independent multi-reviewer assessment produced a quality score of 4.5/10.

3 Results

12 papers retrieved. 10 claims extracted; 2 independently verified. Quality review score: 4.5/10.

4 Limitations

This report is a machine-generated literature synthesis and does not constitute original research. Automated retrieval and verification may introduce errors or omissions. Review scores reflect automated assessment, not human peer review. Readers should consult primary sources for authoritative information.

5 Extracted Claims

Claim	Verified	Confidence
INT8 achieves up to 58$\times$ throughput improvement over CPU baselines.	×	0.13
L4 achieves up to 4.4$\times$ higher throughput than T4 while reaching peak efficiency at smaller batch sizes (B=16–32).	✓	0.30
T4 remains competitive for large-batch, throughput-oriented workloads and environments where cost efficiency, power cons	✓	0.15
DEEP-GAP establishes a controlled empirical basis for understanding the transition from CPU-bound inference to contempor	×	0.11
Single-slot, low-power GPUs have emerged as attractive solutions for scalable inference deployment.	×	0.08
ResNet architectures are selected for this study due to their well-established, reproducible benchmark for evaluating co	×	0.04
ResNet models provide a controlled setting for analyzing the impact of numerical precision and batch-level parallelism o	×	0.07
Deep neural networks have become the dominant approach for a wide range of applications, including computer vision and n	×	0.07
T4 introduces Tensor Cores optimized for mixed-precision inference, supporting FP16 and INT8 acceleration.	×	0.10
L4 introduces substantial architectural enhancements, including increased CUDA core counts, expanded L2 cache capacity,	×	0.10

References

- http://arxiv.org/abs/2604.14552v2
- http://arxiv.org/abs/2509.25716v1
- http://arxiv.org/abs/2602.09439v1