Scalability of Batch-Ensemble BE-SNNs on FPGA and GPU Architectures

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Abstract

This report synthesises findings from 14 peer-reviewed papers addressing the following research question: How does the scalability of the batch-ensemble mechanism in BE-SNNs on FPGA-based hardware compare to GPU-based implementations in terms of throughput and energy efficiency when processing. 15 claims were extracted from source literature; 0 were independently verified against retrieved documents. An automated multi-reviewer quality assessment produced a score of 2.3/10. This report is a machine-generated literature synthesis and does not constitute original research.

1 Introduction

This paper examines: NeuroCoreX: An Open-Source FPGA-Based Spiking Neural Network Emulator with On-Chip Learning. Research question: How does the scalability of the batch-ensemble mechanism in BE-SNNs on FPGA-based hardware compare to GPU-based implementations in terms of throughput and energy efficiency when processing large-scale tabular benchmarks?.

2 Methodology

Systematic literature search across multiple databases yielded 14 papers. Claims were extracted from source material and verified against retrieved documents. An independent multi-reviewer assessment produced a quality score of 2.3/10.

3 Results

14 papers retrieved. 15 claims extracted; 0 independently verified. Quality review score: 2.3/10.

4 Limitations

This report is a machine-generated literature synthesis and does not constitute original research. Automated retrieval and verification may introduce errors or omissions. Review scores reflect automated assessment, not human peer review. Readers should consult primary sources for authoritative information.

5 Extracted Claims

Claim	Verified	Confidence
NeuroCoreX uses 3-bit fixed-point resolution per synapse.	×	0.03
Integrating 3-bit fixed-point models may slightly increase logic complexity.	×	0.03
Integrating 3-bit fixed-point models could significantly reduce BRAM usage.	×	0.02
NeuroCoreX features a modular VHDL design.	×	0.05
NeuroCoreX supports real-time STDP (Spike-Timing-Dependent Plasticity) learning.	×	0.14
SNN execution on NeuroCoreX aligns closely with software simulations in SuperNeuroMAT.	×	0.04
NeuroCoreX is an open-source tool.	×	0.14
NeuroCoreX is capable of performing all computations that a CPU/GPU can perform.	×	0.08
NeuroCoreX supports general-purpose computing workloads in addition to SNN-based AI workloads.	×	0.05
Programming and configuring NeuroCoreX is performed through a UART interface.	×	0.11
Programming and configuring NeuroCoreX is performed through a simple Python module.	×	0.09
The manuscript evaluates NeuroCoreX performance on the DIGITS dataset.	×	0.02
The DIGITS dataset is sourced from the UCI Machine Learning Repository (1998).	×	0.05
NeuroCoreX is designed to emulate brain-like computation on reconfigurable FPGA hardware using a digital circuit approac	×	0.05
The NeuroCoreX system architecture is built around three fundamental components: neurons, synapses, and an unspecified t	×	0.03

References

- http://arxiv.org/abs/2506.14138v1
- http://arxiv.org/abs/2107.13500v1
- http://arxiv.org/abs/2001.10696v5